1. A method of fabricating a contact structure for an integrated circuit, comprising:

providing a semiconductor substrate having a lower bulk insulator layer thereupon, a dielectric layer upon the lower bulk insulator layer, and a conductor layer upon the dielectric layer;

forming a dielectric layer on the lower bulk insulator layer;

forming a conductor layer upon the dielectric layer;

forming a first insulator layer upon the conductor layer;

forming a second insulator layer upon the first insulator layer, said second insulator layer having a top surface and having a thickness greater than that of the first insulator layer;

selectively removing the first and second insulator layers so as to form a opening defined by the lower bulk insulator layer, the dielectric layer, the conductor layer, and the first and second insulator layers, the opening terminating at a bottom surface within the lower bulk insulator layer above the semiconductor substrate;

forming a sleeve insulator layer upon the top surface of said second insulator layer and within said opening so as to make contact with each of the lower bulk insulator layer, the dielectric layer, the conductor layer, and the first and second insulator layers;

removing the sleeve insulator layer from the bottom surface within the lower bulk insulator layer above the semiconductor substrate, from the top surface of the second insulator layer, such that the sleeve insulator layer has a terminus at an interface between the first and second insulator layers, and extends to an opposite terminus that is above the semiconductor substrate, within the lower bulk insulator layer, and below the dielectric layer; and

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removing material of the lower bulk insulator layer to expose a contact on the semiconductor substrate.

2. A method according to Claim 1, wherein at least one of removing the sleeve insulator layer and removing material of the lower bulk insulator layer comprises etching.

3. A method according to Claim 1, further comprising forming a conductive structure in contact with each of the sleeve insulator layer, the contact on the semiconductor substrate, and a sidewall of the lower bulk insulator layer that is situated in between the contact on the semiconductor substrate and the sleeve insulator layer.

4. A method according to Claim 3, wherein the conductive structure has an end comprising at least one refractory metal silicide, said end of said conductive structure being situated upon the contact on the semiconductor substrate.

5. A method according to Claim 3, wherein the conductive structure comprises at least one material selected from the group consisting of tungsten, titanium/titanium nitride/tungsten, titanium/tungsten, aluminum, copper, a refractory metal silicide with aluminum, and a refractory metal silicide with copper.

6. A method as defined in Claim 1, wherein said sleeve insulator layer comprises at least one material selected from the group consisting of Ta_2O_5 and Si_3N_4.

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7. A method of fabricating a contact structure for an integrated circuit, comprising:

providing a semiconductor substrate having a capacitor storage node thereon and having an active region therein that is adjacent to a transistor on said semiconductor substrate, and further having a lower bulk insulator layer upon the active area, the transistor, and the semiconductor substrate, a capacitor dielectric layer upon the lower bulk insulator layer and upon the capacitor storage node, a cell plate conductor layer upon the capacitor dielectric layer, and a cell plate insulator layer upon the cell plate conductor layer;

forming an upper bulk insulator layer upon the cell plate insulator layer, said upper bulk insulator layer having a top surface and a thickness that is greater than that of the cell plate insulator layer;

etching a opening defined by the lower bulk insulator layer, the capacitor dielectric layer, the cell plate conductor layer, the cell plate insulator layer, and the upper bulk insulator layer, the opening terminating at a bottom surface within the lower bulk insulator layer above the semiconductor substrate;

depositing a sleeve insulator layer upon the top surface of said upper bulk insulator layer and within said opening so as to make contact with each of the lower bulk insulator layer, the capacitor dielectric layer, the cell plate conductor layer, and the cell plate insulator layer;

etching the sleeve insulator layer from the bottom surface within the lower bulk insulator layer above the semiconductor substrate, from the top surface of the upper bulk insulator layer, such that the sleeve insulator layer has a terminus at an interface between the upper bulk insulator layer and the cell plate insulator layer, and extends to an opposite terminus that is above the semiconductor substrate, within the lower bulk insulator layer, and below the capacitor dielectric layer;

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etching the lower bulk insulator layer selective to the sleeve insulator layer to expose the active region on the semiconductor substrate;

depositing a conductive plug in contact with each of the sleeve insulator layer, the active region on the semiconductor substrate, and a sidewall of the lower bulk insulator layer that is situated in between the contact on the semiconductor substrate and the sleeve insulator layer, wherein the conductive plug has an end comprising a refractory metal silicide, said end of said conductive plug being situated upon the contact on the semiconductor substrate.

8. The method as defined in Claim 7, further comprising:

forming an electrically conductive bit line in contact with said conductive plug.

9. The method as defined in Claim 7, wherein the conductive plug is at least partially circumscribed by and is in contact with said sleeve insulator layer.

10. The method as defined in Claim 7, wherein said sleeve insulator layer comprises at least one material selected from the group consisting of Ta_2O_5 and Si_3N_4.

11. A method of fabricating a contact structure for an integrated circuit, comprising:

providing a semiconductor substrate having a capacitor storage node thereon, a contact plug on the semiconductor substrate, a lower bulk insulator layer upon the semiconductor substrate, a capacitor dielectric layer upon the lower bulk insulator layer and upon the capacitor storage node, a cell plate conductor layer upon the capacitor dielectric layer, and a cell plate insulator layer having a thickness upon the cell plate conductor layer;

forming an upper bulk insulator layer having a thickness upon the cell plate insulator layer, wherein said thickness of said upper bulk insulator layer is greater than that of the cell plate insulator layer, said upper bulk insulator layer having a top surface;

forming a opening defined by the lower bulk insulator layer, the capacitor dielectric layer, the cell plate conductor layer, the cell plate insulator layer, and the upper bulk insulator layer, the opening terminating at a bottom surface within the lower bulk insulator layer above the semiconductor substrate;

depositing a sleeve insulator layer upon the top surface of said upper bulk insulator layer and within said opening so as to make contact with each of the lower bulk insulator layer, the capacitor dielectric layer, the cell plate conductor layer, and the cell plate insulator layer;

etching the sleeve insulator layer from the bottom surface within the lower bulk insulator layer above the semiconductor substrate, from the top surface of the upper bulk insulator layer, such that the sleeve insulator layer has a terminus at an interface between the upper bulk insulator layer and the cell plate insulator layer, and extends to an opposite terminus that is above the semiconductor substrate, within the lower bulk insulator layer, and below the capacitor dielectric layer;

etching the lower bulk insulator layer to expose the contact plug on the semiconductor substrate;

depositing an electrically conductive bit line contact extending from the sleeve insulator layer to terminate at the contact plug, the contact plug extending from the electrically conductive bit line contact to the contact on said semiconductor substrate, wherein the electrically conductive bit line is in contact with the sleeve insulator layer and a sidewall of the lower bulk insulator layer that is situated in between the contact plug and the sleeve insulator layer.

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12. A method of fabricating a contact structure for an integrated circuit, comprising:

providing a semiconductor substrate having thereon a capacitor storage node, a transistor on the semiconductor substrate, the transistor having a gate electrode, a lower bulk insulator layer upon the semiconductor substrate and upon the transistor, a capacitor dielectric layer upon the lower bulk insulator layer and upon the capacitor storage node, a cell plate conductor layer upon the capacitor dielectric layer, and a cell plate insulator layer upon the cell plate conductor layer;

forming an upper bulk insulator layer upon the cell plate insulator layer, said cell plate insulator layer having a thickness that is less than that of the upper bulk insulator layer, said upper bulk insulator layer having a top surface;

forming a opening defined by the lower bulk insulator layer, the capacitor dielectric layer, the cell plate conductor layer, the cell plate insulator layer, and the upper bulk insulator layer, the opening terminating at a bottom surface within the lower bulk insulator layer above the semiconductor substrate;

depositing a sleeve insulator layer upon the top surface of said upper bulk insulator layer and within said opening so as to make contact with each of the lower bulk insulator layer, the capacitor dielectric layer, the cell plate conductor layer, and the cell plate insulator layer;

etching the sleeve insulator layer from the bottom surface within the lower bulk insulator layer above the semiconductor substrate, from the top surface of the upper bulk insulator layer, such that the sleeve insulator layer has a terminus at an interface between the upper bulk insulator layer and the cell plate insulator layer, and extends to an opposite terminus that is above the semiconductor substrate, within the lower bulk insulator layer, and below the capacitor dielectric layer;

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etching the lower bulk insulator layer and the transistor to expose the gate electrode;

depositing an electrically conductive bit line contact extending from the sleeve insulator layer to terminate at the gate electrode, wherein the electrically conductive bit line is in contact with the sleeve insulator layer and a sidewall of the lower bulk insulator layer that is situated in between the gate electrode and the sleeve insulator layer.

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13. A method of fabricating a contact structure for an integrated circuit, comprising:

providing a semiconductor substrate having a lower bulk insulator layer and a capacitor storage node upon thereupon, and further having a capacitor dielectric layer upon the lower bulk insulator layer on the capacitor storage node, a cell plate conductor layer upon the capacitor dielectric layer, and a cell plate insulator layer upon the cell plate conductor layer:

forming an upper bulk insulator layer upon the cell plate insulator layer, said upper bulk insulator layer having a top surface and a thickness that is greater than that of said cell plate insulator layer;

selectively removing each of the upper bulk insulator layer, the lower bulk insulator layer, the capacitor dielectric layer, the cell plate conductor layer, and the cell plate insulator layer to define an opening that terminates at a bottom surface within the lower bulk insulator layer above the semiconductor substrate;

forming a sleeve insulator layer upon the top surface of said upper bulk insulator layer and within said opening so as to make contact with each of the lower bulk insulator layer, the capacitor dielectric layer, the cell plate conductor layer, and the cell plate insulator layer;

selectively removing the sleeve insulator layer to have a terminus at an interface between the upper bulk insulator layer and the cell plate insulator layer, and an extension to an opposite terminus that is above the semiconductor substrate, within the lower bulk insulator layer, and below the capacitor dielectric layer; and

removing material of the lower bulk insulator layer to expose a contact on the semiconductor substrate.

14. A method according to Claim 13, wherein at least one of selectively removing the sleeve insulator layer and removing material of the lower bulk insulator layer comprises etching.

15. A method according to Claim 13, further comprising forming a conductive plug in contact with each of the sleeve insulator layer, the contact on the semiconductor substrate, and a sidewall of the lower bulk insulator layer that is situated in between the contact on the semiconductor substrate and the sleeve insulator layer.

16. A method according to Claim 15, wherein the conductive plug has an end comprising a refractory metal silicide, said end of said conductive plug being situated upon the contact on the semiconductor substrate.

17. A method as defined in Claim 13, wherein said sleeve insulator layer comprises at least one material selected from the group consisting of Ta_2O_5 and Si_3N_4..

18. A method as defined in Claim 15, wherein said conductive plug comprises:

a electrically conductive bit line contact extending from the sleeve insulator layer to terminate at a contact plug, the contact plug extending from the electrically conductive bit line contact to the contact on said semiconductor substrate.

19. A method according to Claim 15, wherein the conductive plug comprises at least one electrically conductive material selected from the group consisting of tungsten, titanium/titanium nitride/tungsten, titanium/tungsten, aluminum, copper, a refractory metal silicide with aluminum, and a refractory metal silicide with copper.

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20. A method of fabricating a contact structure for an integrated circuit, comprising:

providing a semiconductor substrate having a lower bulk insulator layer and a capacitor storage node thereupon, and further having, a capacitor dielectric layer upon the capacitor storage node, a cell plate conductor layer upon the capacitor storage node and above the lower bulk insulator layer, and a cell plate insulator layer upon the cell plate conductor layer;

forming an upper bulk insulator layer upon the cell plate insulator layer, the upper bulk insulator layer having a top surface and a thickness that is greater than that of the cell plate insulator layer;

forming an opening that is defined by each of the lower bulk insulator layer, the capacitor dielectric layer, the cell plate conductor layer, the cell plate insulator layer, and the upper bulk insulator layer, the opening extending towards the semiconductor substrate and terminating at a bottom surface within the lower bulk insulator layer above the semiconductor substrate;

forming a sleeve insulator layer upon said upper bulk insulator layer and within said opening so that the sleeve insulator layer makes contact with each of the lower bulk insulator layer, the cell plate conductor layer, and the cell plate insulator layer;

selectively removing the sleeve insulator layer so as to have a terminus at an interface between the upper bulk insulator layer and the cell plate insulator layer and an extension to an opposite terminus that is within the lower bulk insulator layer and above the semiconductor substrate; and

removing the lower bulk insulator layer from the bottom surface within the lower bulk insulator layer above the semiconductor substrate to expose a contact on the semiconductor substrate.

21. A method according to Claim 20, further comprising forming a conductive plug in contact with each of the sleeve insulator layer, the contact on the semiconductor substrate, and a sidewall of the lower bulk insulator layer that is situated in between the contact on the semiconductor substrate and the sleeve insulator layer.

22. The method as defined in Claim 20, further comprising:

forming an electrically conductive plug upon the contact and extending through the sleeve insulator layer.

23. The method as defined in Claim 20, wherein the opposite terminus of the sleeve insulator layer is between the cell dielectric layer and the semiconductor substrate.

24. The method as defined in Claim 22, further comprising:

forming an electrically conductive bit line in contact with said electrically conductive plug.

25. The method as defined in Claim 22, wherein the electrically conductive plug is at least partially circumscribed by and is in contact with said sleeve insulator layer.

26. The method as defined in Claim 20, wherein said sleeve insulator layer comprises at least one material selected from the group consisting of Ta_2O_5 and Si_3N_4.

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27. A method of fabricating a contact structure for an integrated circuit, comprising:

providing a semiconductor substrate having a lower bulk insulator layer and a capacitor storage node thereupon, and further having, a capacitor dielectric layer upon the capacitor storage node and upon the lower bulk insulator layer, a cell plate conductor layer upon the capacitor dielectric layer, and a cell plate insulator layer upon the cell plate conductor layer;

forming an upper bulk insulator layer upon the cell plate insulator layer, wherein the thickness of the upper bulk insulator layer is greater than that of the cell plate insulator layer;

selectively removing each of the upper bulk insulator layer, the cell plate insulator layer, the cell plate conductor layer, the capacitor dielectric layer, and the lower bulk insulator layer so as to form a opening terminating at a bottom surface within the lower bulk insulator layer above the semiconductor substrate;

depositing a sleeve insulator layer upon said upper bulk insulator layer and within said opening so as to make contact with each of the lower bulk insulator layer, the capacitor dielectric layer, the cell plate conductor layer, and the cell plate insulator layer;

selectively removing the sleeve insulator layer such that a remaining portion thereof extends from a terminus at an interface between the upper bulk insulator layer and the cell plate insulator layer to an opposite terminus within the lower bulk insulator layer and above the semiconductor substrate;

selectively removing the lower bulk insulator layer to create a contact hole defined by the sleeve insulator layer and the lower bulk insulator layer and to expose a contact on the semiconductor substrate; and

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forming a conductive plug in the contact hole upon the contact on the semiconductor substrate, said sleeve insulator layer electrically insulating the conductive plug from the cell plate conductor layer.

28. The method as defined in Claim 27, wherein the electrically conductive plug is at least partially circumscribed by and is in contact with said sleeve insulator layer.

29. The method as defined in Claim 27, wherein said sleeve insulator layer comprises at least one material selected from the group consisting of Ta_2O_5 and Si_3N_4..

30. The method as defined in Claim 27, further comprising:

forming an electrically conductive bit line in contact with said electrically conductive plug.

31. The method as defined in Claim 27, wherein the opposite terminus of the sleeve insulator layer is between the cell dielectric layer and the semiconductor substrate.

32. A method of fabricating a contact structure for an integrated circuit, comprising:

providing a semiconductor substrate having a lower bulk insulator layer and a capacitor storage node thereupon, and further having a capacitor dielectric layer upon the capacitor storage node and upon the lower bulk insulator layer, a cell plate conductor layer upon the capacitor dielectric layer, and a cell plate insulator layer upon the cell plate conductor layer;

forming an upper bulk insulator layer upon the cell plate insulator layer;

selectively removing each of the upper bulk insulator layer, the cell plate insulator layer, the lower bulk insulator layer, the capacitor dielectric layer, and the cell plate conductor layer to define an opening terminating at a bottom surface within the lower bulk insulator layer above the semiconductor substrate;

depositing a sleeve insulator layer upon said upper bulk insulator layer and within said opening so as to make contact with each of the lower bulk insulator layer, the capacitor dielectric layer, the cell plate conductor layer, and the cell plate insulator layer;

selectively removing the sleeve insulator layer such that a remaining portion thereof extends from a terminus at an interface between the upper bulk insulator layer and the cell plate insulator layer to an opposite terminus that is within the lower bulk insulator layer and above the semiconductor substrate;

selectively removing material from the lower bulk insulator layer to create a contact hole extending from the upper bulk insulator layer through the sleeve insulator layer and the lower bulk insulator layer to expose a contact on the semiconductor substrate; and

forming a conductive plug in the contact hole upon the contact on the semiconductor substrate and extending to the upper bulk insulator layer, said sleeve

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insulator layer electrically insulating the conductive plug from the cell plate conductor layer.

33. The method as defined in Claim 32, wherein the conductive plug is at least partially circumscribed by and is in contact with said sleeve insulator layer.

34. The method as defined in Claim 32, wherein said sleeve insulator layer comprises at least one material selected from the group consisting of Ta_2O_5 and Si_3N_4..

35. The method as defined in Claim 32, further comprising:

forming an electrically conductive bit line in contact with said conductive plug.

36. The method as defined in Claim 32, wherein the opposite terminus of the sleeve insulator layer is between the cell dielectric layer and the semiconductor substrate.

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37. A method of fabricating a contact structure for an integrated circuit, comprising:

providing a semiconductor substrate having an active region therein, a capacitor storage node upon the active region, a capacitor dielectric layer upon the capacitor storage node, and a cell plate conductor layer upon the capacitor dielectric layer;

forming a cell plate insulator layer upon the cell plate conductor layer;

forming a upper bulk insulator layer upon the cell plate insulator layer, wherein the upper bulk insulator layer is greater in thickness than the cell plate insulator layer;

forming a contact hole extending through the upper bulk insulator layer, the cell plate insulator layer, the cell plate conductor layer, the capacitor dielectric layer, and the capacitor storage node to terminate at the active region;

forming a sleeve insulator layer within the contact hole, the sleeve insulator layer extending from a terminus at an interface between the upper bulk insulator layer and the cell plate insulator layer and an opposite terminus that is below the capacitor dielectric layer and above the semiconductor substrate; and

forming an electrically conductive plug extending through the sleeve insulator layer to make contact with the active region and the capacitor storage node, the electrically conductive plug being electrically insulated from the cell plate conductor layer by the sleeve insulator layer.

38. The method as defined in Claim 37, further comprising, prior to forming said electrically conductive plug:

forming a first transistor upon the semiconductor substrate;

forming a second transistor upon the semiconductor substrate, and

wherein forming said electrically conductive plug further comprises forming a first portion of the electrically conductive plug so as to be is situated between the first and second transistors and between the semiconductor substrate and the sleeve insulator layer.

39. The method as defined in Claim 38, wherein the first portion of the electrically conductive plug is enclosed within the sleeve insulator layer.

40. The method as defined in Claim 37, wherein the electrically conductive plug is at least partially circumscribed by and is in contact with said sleeve insulator layer.

41. The method as defined in Claim 37, wherein said sleeve insulator layer comprises at least one material selected from the group consisting of Ta_2O_5 and Si_3N_4.

42. The method as defined in Claim 37, further comprising:

forming an electrically conductive bit line in contact with said electrically conductive plug.

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43. A method of fabricating an integrated circuit that includes a semiconductor substrate having an active region therein, a capacitor storage node upon the active region, a capacitor dielectric layer upon the capacitor storage node, a cell plate conductor layer upon the capacitor dielectric layer, a cell plate insulator layer upon the cell plate conductor layer, and an upper bulk insulator layer upon the cell plate insulator layer, the method comprising:

forming a contact hole extending through the upper bulk insulator layer, the cell plate insulator layer, the cell plate conductor layer, the capacitor dielectric layer, and the capacitor storage node to terminate at the active region;

forming a sleeve insulator layer within the contact hole, the sleeve insulator layer extending from a terminus at an interface between the upper bulk insulator layer and the cell plate insulator layer and an opposite terminus that is below the capacitor dielectric layer and above the semiconductor substrate;

forming an electrically conductive plug extending through the sleeve insulator layer to make contact with the active region and the capacitor storage node, the electrically conductive plug being electrically insulated from the cell plate conductor layer by the sleeve insulator layer.